In the claims:

Please amend the claims as follows:

Claims 1-10 (canceled).

11. (currently amended) A passenger transit car comprising:

a) at least one car drive motor;

b) at least one ~~a first plurality of~~ solenoid~~s~~;

c) at least one ~~a second plurality of~~ mechanical switch~~es~~;

d) at least one ~~a third plurality of~~ motor~~s~~ for moving doors on said passenger transit car;

e) an electrical control unit comprising:

i) a mother board located in said control unit having at least one ~~a fourth plurality of daughter~~ board~~s~~ wherein said electrical control unit is connected to said at least one ~~first plurality of~~ solenoid~~s~~, to said at least one ~~second plurality of~~ mechanical switch~~es~~, and to said at least one ~~third plurality of~~ motor~~s~~ for moving doors on said passenger transit car;

ii) a self-locking memory circuit located in said control unit for a tristate ~~tri state~~ data bus having multiple bit lines, said self-locking memory circuit comprising:

A) a non-clocked, non-inverting amplifier chip for connection to one of said bit lines;

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B) a resistor having a predetermined electrical resistance connected across said non-clocked, non-inverting amplifier chip; and

C) wherein said self-locking memory circuit has upper and lower voltage thresholds that cause said self-locking memory circuit to change states when a level of voltage applied to said self-locking memory circuit passes through one of said thresholds.

12. (previously added) A passenger transit car according to claim 11 wherein said passenger transit car ~~self-locking memory circuit~~ includes:

a central processing unit;

a Digital Signal Processor (DSP) for transceiving discrete electrical inputs; and

a tri state data bus electrically connecting said Digital Signal Processor to said central processing unit, said Digital Signal Processor and said central processing unit having different clock rates for accessing said tristate ~~tri state~~ data bus.

13. (previously added) A passenger transit car according to claim 12 ~~11~~ wherein said passenger transit car ~~self-locking memory circuit~~ includes:

a Complex Programmable Logic Device (CPLD) for transceiving discrete electrical signals; and

wherein said tri state data bus electrically interconnects said central processing unit, said Digital Signal Processor, and said Complex Programmable Logic Device, said Digital Signal Processor and said Complex Programmable Logic Device having clock rates for accessing said tristate ~~tri state~~ data bus that are different from a clock rate at which said central processing unit accesses said tri state data bus.

Claim 14(canceled).